UCSD ECE 111 – Advanced Digital Design Project (Fall 2018)

General:
- Class section/meeting times
  - Lectures: Tues/Thurs 2:00-3:20PM
    Location: Pepper Canyon Hall, PCYNH-121
  - Discussion: Wed 2:00-2:50PM
    Location: Warren Lecture Hall, WLH-2111
  - Office Hours: Tues 12-1:50PM or by e-mail appointments
    Location: Jacobs Hall, EBU1-6104
- Instructor
  - Prof. Farinaz Koushanfar
  - Office: Jacobs Hall, EBU1-6104
  - Office phone: 858-246-0251
  - Email: farinaz@ucsd.edu
- TAs
  - Siam Umar Hussain s2hussai@eng.ucsd.edu
- Class webpage:
  - TritonEd
  - http://eceweb.ucsd.edu/~fkoushanfar/teaching/fall2018/ece111/

Objectives:
In this course, students will learn about automated digital design. They will learn to utilize a hardware description language (HDL) in the digital design process. The language of choice is Verilog. Emphasis is on system level concepts and high-level design, and the language syntax will be presented to support the realization of the presented concepts. The students will get to design, synthesize (compile), simulate, and optimize the digital design, on a real hardware simulation platform. More specifically, a commercial computer aided design tool will be used to design a series of increasingly sophisticated designs on field programmable gate arrays (FPGAs).

Prerequisites:
- Familiarity with at least one programming language such as C, C++, Java, Python, etc.
- ECE 25 or CSE 140. Specifically, familiarity with Boolean Algebra, logic gates, combinational circuits, sequential circuits, memory forms, finite state machines, and timing analysis.

Textbook and Design tool:
- Course textbook:
  - David Money Harris and Sarah L. Harris, Digital Design and Computer Architecture, 2nd Edition © 2012 by Elsevier Inc. (Chapter 4)
- More readings (for interested students):
Steven W. Smith, Digital signal processing: a practical guide for engineers and scientists
- Design tool: Xilinx Vivado
  - Xilinx Vivado is a tool for synthesis ("compilation") and analysis of HDL designs on Xilinx FPGAs
  - Enables developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design’s reaction to different stimuli, and configure the target device with the programmer

**Assignments, midterms and final project**

There will be 5 homeworks and assignments for this course, and one final project. The assignments are designed to help you with parts of the final project. The assignments will have to be turned in on-time. The assignment evaluation is based on test-benches. Some of the assignment solutions may not be posted – if they are an integral part of the final project.

- Each assignment must be solved by the exact turn-in date for each assignment will be provided with the assignment.
- Assignments will be posted on the course website, and announced in the discussion section.
- There is no late policy in this course. Homework and Project assignments have to be posted on TritonEd before the due deadline of each assignment.
- Late assignments because of technical issues are not accepted.
- The first three assignments are individual assignments and must be completed independently by the students. The Forum on the course web site can be used to discuss the assignments within the limits of the Honor Code Policy provided below.
- The rest of the assignments and final project will be done in groups of 2 students.
- Accommodations available for students with disabilities, religious and ethnic holidays, and illness (with proper documentation)
Grading
The final grade breakdown is as follows:
- On-time Assignment/Participation: 10%
- Assignments: 40%
- Final project (teams of two): 50%

Student Code of Conduct
- Adherence to UCSD student code of conduct is expected in all phases of this course: https://students.ucsd.edu/sponsor/student-conduct/regulations/22.00.html
- Violations will be reported to the Student Conduct Office

Tentative schedule:

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*subject to change